Remarks

I. Status of claims

Claims 1-20 are pending.

The dependency of claim 16 has been corrected.

The Examiner has indicated that claims 5-11, 13-14, 16, and 19-20 would be allowable if rewritten in independent form.

II. Claim rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1-4, 12, 15, 17, and 18 under 35 U.S.C. § 102(e) over Mirov (U.S. 6,608,476).

A. Independent claim 1

Independent claim 1 recites:

> Claim 1 (original): A device, comprising:
>
> a sleep recovery circuit operable to transition from a first signal detection mode to a second signal detection mode in response to detection of a first signal characteristic in an input signal, and to transition from the second signal detection mode to a third operational mode in response to detection in the input signal of a second signal characteristic different from the first signal characteristic.

In support of the rejection of claim 1, the Examiner has stated that:

> ... Mirov teaches a device [200 of Fig. 2], comprising: a sleep recovery circuit operable to transition from a first signal detection mode to a second signal detection mode [transition from idle mode reduced power mode] in response to detection of a first signal characteristic in an input signal [detecting that bits 300 and 302 of register 220 of fig. 3 are 01, see col. 6, table 1], and to transition from the second signal detection mode to a third operational mode [transition from reduced power mode to normal mode] in response to detection in the input signal of a second signal characteristic different from the first signal characteristic [detecting that bits 300 and 302 of register 220 of fig. 3 are 00, see col. 6, table 1].

Mirov's computer system 200, however, does not operate in the manner described by the Examiner in support of the rejection of claim 1. In particular, contrary to the Examiner's statement, Mirov's computer system 200 does not transition from idle mode to reduced power mode *in response to* detecting that bits 300 and 302 of register 220 are set to 01, nor does it transition from the reduced power mode to normal mode *in response to* detecting that bits 300 and 302 of register 220 are 00. In col. 6, line 66 - col. 7, line 13, Mirov explains that (emphasis added):

> The register bits 300, 302 are set to the desired value by the power controller 218 of the BBC 216. That is, prior to switching between the various operating modes, software operating on the computer system 200 performs a write operation into each of the registers 220 to set the values of the bits 300, 302 to the desired level in anticipation of an upcoming switch in operating modes. For example, assume that the computer system 200 is presently operating in the normal mode but that a relatively low load is currently being placed on the computer system 200, such that the computer system 200 may be switched to the reduced power operating mode. Software, which is executed by one or both of the CPUs 202, 204 writes the binary value 01 into the register 220 at the bits 300, 302 to indicate that the component 202 should switch to the reduced power operating mode during the next transition.

Thus, the values of the register bits 300, 302 on a register 220 of a particular one of the components 202-214 merely indicate the operating mode to which the component will switch "during the next transition." None of the components 202-214 transitions between the operating modes in response to detection of the values of the register bits. Instead, in accordance with Mirov's teachings, the components 202-214 transition from one operating mode to another only in response to detecting that the DC voltage level of the Change signal 408 has been set to a low value (see col. 8, lines 23-42, and FIG. 4). Consequently, in accordance with Mirov's teachings, each of the components 202-214 transitions from one operating mode to another only in response to the detection of the same signal characteristic in the Change signal 408: namely, a low DC voltage level in the Change signal 408.

For at least this reason, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(e) over Mirov should be withdrawn.

In addition, the detection of the values of the register bits 300, 302 involves detecting changes in the DC voltage levels of two different input signals (i.e., the register bits 300, 302). Therefore, contrary to the Examiner's statement, the detecting of the register bits with

values 00 and 01 does not constitute detecting a first signal characteristic in an input signal and detecting a second signal characteristic different from the first signal characteristic in the same input signal.

For at least this additional reason, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(e) over Mirov should be withdrawn.

Furthermore, there is no basis for the Examiner's assertion that the transition of Mirov's computer system 200 from the idle operating mode to the reduced power operating mode constitutes a "transition from a first signal detection mode to a second signal detection mode," as recited in claim 1. In accordance with Mirov's teachings, the transition from the idle operating mode to the reduced power operating mode merely involves changing the clock frequency from a low frequency (e.g., 1/32 of the full clock frequency) to a higher frequency (e.g., 1/2 the full clock frequency). Mirov does not teach or suggest anything that would have led one skilled in the art at the time the invention was made to believe that such changes in the clock frequency involved changing the signal detection modes of any of the components 202-214. Indeed, Mirov does not teach or suggest anything about signal detection modes.

For at least this additional reason, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(e) over Mirov should be withdrawn.

B. Claims 2-4, 12, 15, and 17

Each of claims 2-4, 12, 15, and 17 incorporates the features of independent claim 1 and therefore is patentable over Mirov for at least the same reasons explained above.

C. Independent claim 18

Independent claim 18 recites features that essentially track the pertinent features discussed above in connection with independent claim 1 and, therefore, is patentable over Mirov for at least the same reasons explained above.

III. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-3718.

Respectfully submitted,

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